EXEMPLAR LOGIC

Product Comparison Table

	VHDL Discovery Kit	Galileo	Leonardo
Inputs	VHDL Only	VHDL, Verilog, Netlists	VHDL, Verilog, Netlists
Optimization & Synthesis			
• **Architecture Specific Optimization**	X	X	X
• **Hierarchy Support**	Automatically flattens	Automatically flattens	Preserve and manipulate
• **Browse Hierarchy**			X
• **Synthesis Control**	Set global constraints for the entire design at the beginning of the run	Set global constraints for the entire design at the beginning of the run	Interactive manipulate optimizations Constraints for different portions separately or for the entire design
• **Critical path optimization**	--	--	Available with Leonardo Timing Module
• **Delay Modeling**	piece-wise linear, linear	piece-wise linear, linear	non-linear (look-up table), piece wise linear, & linear
• **Fast synthesis option**	Quick estimate of size and speed	Quick estimate of size and speed	up to 25 times faster than full opt.
• **Retargeting Support**	--	X	X

	VHDL Discovery Kit	Galileo	Leonardo
User Interface			
• **Interactive control over optimization**	--	--	X
• **Automated Flow**	X	X	X
• **Guided assistance for new users**	--	--	Flow guide
• **Schematic Viewer**	--	Galileo Time Explorer option	X
• **Scripting**	--		Tcl/TK-based scripting & customization Command capture and record
Outputs	EDIF or XNF for FPGA vendor place & route tools	VHDL, Verilog, RTL VHDL, netlist	VHDL, Verilog, RTL VHDL, netlist

	VHDL Discovery Kit	Galileo	Leonardo
Simulation		Model Technology V-System and V-Log option and links to other simulators	Model Technology V-System and V-Log option and links to other simulators

Design Verification	-	Galileo Time Explorer Option	Leonardo Timing Module
Static Timing Analysis	--	X	X
Backannotation	--	SDF and XNF	SDF and XNF
Critical path reporting	--	X	X
Vital Libraries	--	X	X

Supported Platforms	Windows95 & Windows NT	Windows95, Windows NT Sun OS, Solaris HP-UX	Windows 95, Windows NT Sun OS, Solaris HP-UX